REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. The foregoing amendments are responsive to the November 13, 2000 Office Action. Applicants respectfully request entry of the requested amendments and reconsideration of the application in view of the following comments.

Amendment to the Drawings

A Request for Drawing Correction is submitted herewith to correct the label 108 in Figure 1D to read 104.

Amendments to the Specification

The specification is amended to define the abbreviation "AFM" as Atomic Force Microscopy.

Response to Claim Objections

Claim 16 is objected to because the word "wet" is spelled incorrectly. Applicants amend Claim 16 herein to correct the spelling.

Response to the Claim Rejections Under 35 U.S.C §§ 102 and 103

Claims 2, 3, and 5-30 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,693,541 issu

to Yamazaki, et al. The rejection asserts that Yamazaki teaches each element of the claims. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of U.S. Patent No. 5,430,320 issued to Lee. The rejection asserts that Yamazaki allegedly teaches each element of the claims except for thin film transistors having lightly doped regions, which is allegedly taught by Lee. Claims 35-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of U.S. Patent No. 6,027,960 issued to Kusumoto, et al. The rejection asserts that Yamazaki allegedly teaches each element of the claims except for having the insulating layer suppress the formation of ridges, which is allegedly taught by Kusumoto. Claims 31-34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Kusumoto in further view of Wolf. The rejection asserts that Yamazaki and Kusumoto allegedly teaches each element of the claims except for the insulating layer being silicon nitride, which is allegedly taught by Wolf.

The present invention is directed toward a semiconductor device having a crystalline semiconductor layer. The crystalline semiconductor layer comprises a channel formation region in which the crystalline semiconductor layer has a ridge on a surface thereof. The ridge is less than 500 Å over the channel formation region.

Conventionally, a ridge might be formed when an exposed surface of a silicon film is subjected to laser irradiation. The ridge may raise the energy level at the interface between the silicon film (the active layer) and the gate insulating film. Thus, the characteristics of the TFTs are deteriorated. Because the ridge in the present invention is less than 500 Å over the channel formation region, the semiconductor device has an excellent interface level between the channel formation region and a gate insulating film.

None of the cited art teaches or suggests a channel formation region in which the crystalline semiconductor layer has a ridge less than 500 Å over the channel formation region. Yamazaki teaches activating a source and a drain region by a laser light. Although Yamazaki thermally crystallizes a semiconductor film having a part to become a channel formation region, Yamazaki does not irradiate a laser light to the part to become the channel formation region. Lee teaches an LDD and Wolf teaches a silicon nitride film, but neither teach laser irradiation.

Kusumoto has a filing date of October 23, 1996. The Japanese priority application of the present application has a filing date of November 30, 1995, prior to the Kusumoto filing date. Thus, Kusumoto is not prior art to the present

application. Applicants will submit an English translation of the Japanese priority application.

In view of the foregoing distinctions, Applicants respectfully submit that independent Claims 2-5, 11, 18, 24, 31, 35, and 40 are patentably distinguished over the cited art. Applicants respectfully submit that Claims 2-5, 11, 18, 24, 31, 35, and 40 are in condition for allowance, and Applicants respectfully request allowance of Claims 2-5, 11, 18, 24, 31, 35, and 40.

Claims 6-10, 12-17, 19-23, 25-30, 32-34, 36-39, and 41-44 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding Claims 2-5, 11, 18, 24, 31, 35, and 40, Applicants respectfully submit that Claims 6-10, 12-17, 19-23, 25-30, 32-34, 36-39, and 41-44 are likewise in condition for allowance. Applicants respectfully request allowance of dependent Claims 6-10, 12-17, 19-23, 25-30, 32-34, 36-39, and 41-44.

Summary

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/12/01

Reg. No. 40,631

Scott C. Harris
Reg. No. 32,030

Fish & Richardson P.C.
4350 La Jolla Village Drive, Suite 500
San Diego, CA 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10099146.doc

Version to Show Changes Made

Paragraph beginning at page 9, line 7 has been amended as follows:

Measurements with an AFM (Atomic Force Microscopy) have revealed that where no capping layer existed as in the prior art techniques, the sizes of the ridges were about 500 Å, and that where a capping layer consisting of the silicon oxide film according to the invention existed, the sizes of the ridges were less than about 200 Å. Generation of the ridges can be suppressed by subjecting the crystalline silicon film to laser annealing while it is capped with the first dielectric film.

In the Claims:

Claims 2, 3, 4, 5, 11, 18, 31, 35, and 40 have been amended as follows:

2. (Amended) A semiconductor device comprising:

a crystalline semiconductor [layer] island comprising silicon over a substrate, said semiconductor island comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

[an insulating layer comprising a thermal oxide of said semiconductor layer, said thermal oxide being provided in contact with a surface of said semiconductor layer and

constituting a part of a gate insulating layer of said semiconductor device,]

a gate insulating film comprising a silicon oxide layer and a silicon nitride layer with said silicon nitride layer provided over said silicon oxide layer,

wherein said silicon oxide layer is provided over said crystalline semiconductor island and has a side aligned with a side of said crystalline semiconductor island, and

wherein said crystalline semiconductor [layer] island has a ridge [less than 500 Å] on [said] a surface of said semiconductor [layer] island, and

wherein said ridge is less than 500 Å over said channel formation region.

3.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon over a substrate, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

an insulating layer comprising a thermal oxide of said semiconductor layer, said thermal oxide being provided in contact with a surface of said semiconductor layer and constituting a part of a gate insulating layer of said semiconductor device; and

a gate electrode provided adjacent to said channel formation region with said gate insulating layer therebetween,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on said surface of said semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

4.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon over a substrate, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region with at least one lightly doped region between said channel formation region and at least one of said source region and said drain region;

an insulating layer comprising a thermal oxide of said semiconductor layer, said thermal oxide being provided in contact with a surface of said semiconductor layer and constituting a part of a gate insulating layer of said semiconductor device; and

a gate electrode provided adjacent to said channel formation region with said gate insulating layer therebetween,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on said surface of said semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

5.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on a surface of said crystalline semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

11.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said

insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on a surface of said crystalline semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

16.(Amended) The device of claim 11 wherein the silicon oxide of said insulating layer is formed by [we] wet oxidation or hydrogen chloride oxidation.

18.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] measured by AFM on a surface of said crystalline semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

24.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] measured by AFM on a surface of said crystalline layer, and

wherein said ridge is less than 500 Å over said channel formation region.

31. (Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on a surface of said crystalline semiconductor layer, [and]

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer comprising silicon nitride is provided on said semiconductor layer, in order to suppress formation of said ridge.

35.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] on a surface of said crystalline semiconductor layer, [and]

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer comprising silicon oxide is provided on said semiconductor layer, in order to suppress formation of said ridge.

40.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge [less than 500 Å] measured by AFM on a surface of said crystalline [and] semiconductor layer, [and]

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer is provided on said semiconductor layer, in order to suppress formation of said ridge.